Course Code: 18EC0431 **R18**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
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QUESTION BANK (DESCRIPTIVE)

Subject with Code: VLSI Design (18EC0431) **Course & Branch**: B.Tech - ECE

Regulation: R18 **Year & Sem:** IV-B.Tech & I-Sem

UNIT –I
INTRODUCTION AND BASIC ELECTRICAL PROPERTIES OF MOS AND Bi-CMOS CIRCUITS

1	**a)**	Enumerate various VLSI Technologies?	[L1] [CO2]	**[2M]**
	b)	Define Threshold Voltage of the MOS transistor.	[L1] [CO2]	**[2M]**
	c)	List the figure of merit of the MOS transistor.	[L1] [CO2]	**[2M]**
	d)	Define Transconductance and Output Conductance.	[L1] [CO2]	**[2M]**
	e)	Discuss about body bias effect in the NMOS Transistor.	[L2] [CO2]	**[2M]**
2	**a)**	Explain working of the NMOS Transistor.	[L2] [CO2]	**[6M]**
	b)	Summarize the evolution of microelectronics.	[L2] [CO1]	**[4M]**
3	**a)**	What is the need of VLSI circuits?	[L1] [CO2]	**[4M]**
	b)	Compare the relative merits of three different forms of pull up for an invertercircuit. Which is the best choice for realization?	[L2] [CO2]	**[6M]**
4	**a)**	Compare CMOS with Bipolar technology in different aspects.	[L2] [CO1]	**[4M]**
	b)	Show the circuit diagram of a simple BiCMOS inverter and explain itsoperation.	[L1] [CO2]	**[6M]**
5		Determine the relationship between I_{ds} & V_{ds} in non-saturated and saturated region.	[L3] [CO2]	**[10M]**
6		Illustrate the steps involved in nMOS fabrication process with neat sketches.	[L2] [CO1]	**[10M]**
7	**a)**	Illustrate about basic MOS transistors.	[L2] [CO1]	**[4M]**
	b)	Explain the steps involved in Bi-CMOS fabrication process.	[L2] [CO1]	**[6M]**
8		Distinguish various pull-up loads used in Inverter Circuit.	[L4] [CO5]	**[10M]**
9		Explain the steps involved in pMOS fabrication process with neat sketches.	[L2] [CO1]	**[10M]**
10	**a)**	Explain the steps involved in p-well CMOS fabrication process with neatsketches.	[L2] [CO1]	**[6M]**
	b)	Define Metal Oxide Semiconductor VLSI Technology.	[L1] [CO1]	**[4M]**
11		Explain the following briefly	[L2] [CO2]	**[10M]**
		(i) Channel length Modulation (ii) Transconductance (iii) Output Conductance (iv) Figure of merit (ω_o)		

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UNIT –II
VLSI CIRCUIT DESIGN PROCESS

1	**a)**	List different MOS layers.	[L1] [CO3]	**[2M]**
	b)	Draw the circuit diagram of CMOS Inverter Circuit.	[L4] [CO3]	**[2M]**
	c)	Illustrate nMOS transistor in λ-based design rule.	[L2] [CO3]	**[2M]**
	d)	Illustrate a contact cut in λ-based design rule.	[L2] [CO3]	**[2M]**
	e)	Illustrate pMOS transistor in 2μm design rule.	[L2] [CO3]	**[2M]**
2	**a)**	Explain the steps involved in VLSI Design flow.	[L2] [CO3]	**[5M]**
	b)	Construct the stick diagram of a 2-input CMOS NAND gate.	[L3] [CO3]	**[5M]**
3	**a)**	What is lambda-based design rules? Explain.	[L1] [CO3]	**[5M]**
	b)	Illustrate design rules for wires and MOS transistors.	[L2] [CO3]	**[5M]**
4	**a)**	Summarize 2μm based design rules with neat sketches.	[L2] [CO3]	**[5M]**
	b)	Draw the layout diagram of NMOS inverter circuit such that both input andoutput points are connected with Polysilicon layer.	[L4] [CO3]	**[5M]**
5	**a)**	Explain about Stick diagram with one example.	[L2] [CO3]	**[5M]**
	b)	Sketch the layout diagram for 2-input CMOS NAND gate.	[L3] [CO3]	**[5M]**
6	**a)**	Explain 2μm design rules for contacts and transistors.	[L2] [CO3]	**[5M]**
	b)	Sketch the layout diagram for CMOS inverter.	[L3] [CO3]	**[5M]**
7	**a)**	Construct stick diagram for $\boldsymbol{Y = \overline{(AB + CD)}}$ in NMOS design style.	[L3] [CO3]	**[5M]**
	b)	Construct the layout diagram for 2-input CMOS NOR gate.	[L3] [CO3]	**[5M]**
8		Construct layout diagram for the logic equations in CMOS logic. (i) $\boldsymbol{Y = \overline{(A + B)C}}$ (ii) Z= $\boldsymbol{\overline{(AB + CD)}E}$	[L3] [CO3]	**[10M]**
9	**a)**	Illustrate λ-design rules for contact cuts.	[L2] [CO3]	**[5M]**
	b)	How a p-MOS transistor forms in lambda-based design rules? Explain.	[L1] [CO3]	**[5M]**
10	**a)**	Illustrate stick diagram of AND-OR-INVERTER in CMOS design Style.	[L2] [CO3]	**[5M]**
	b)	Explain about Implant and demarcation line in stick diagrams with neat sketches.	[L2] [CO3]	**[5M]**
11	**a)**	Construct the stick diagram for 2-input CMOS XOR gate.	[L3] [CO3]	**[5M]**
	b)	Explain different types of MOS layers used in VLSI circuits.	[L2] [CO1]	**[5M]**

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UNIT –III
GATE LEVEL DESIGN & PHYSICAL DESIGN

1	**a)**	Briefly describe Switch logic.	[L1] [CO4]	**[2M]**
	b)	List Alternate gate circuits.	[L1] [CO5]	**[2M]**
	c)	List the Complex gates circuits.	[L1] [CO5]	**[2M]**
	d)	Define Placement in the Physical design.	[L1] [CO5]	**[2M]**
	e)	Define Routing in the geometrical layouts.	[L1] [CO5]	**[2M]**
2	**a)**	Sketch 2 x 1 mux using transmission gates.	[L3] [CO4]	**[5M]**
	b)	Explain the implementation of AOI using CMOS design style with neat sketches.	[L2] [CO4]	**[5M]**
3	**a)**	What is switch logic? Explain with an example.	[L1] [CO4]	**[5M]**
	b)	Explain about pass transistors logic with an example.	[L2] [CO4]	**[5M]**
4	**a)**	What is pseudo NMOS logic? Explain with an example	[L1] [CO4]	**[5M]**
	b)	Construct 2-input NAND gate by using pseudo NMOS logic.	[L3] [CO4]	**[5M]**
5	**a)**	Explain dynamic CMOS logic circuit with an example.	[L2] [CO4]	**[5M]**
	b)	List the advantages & disadvantages of dynamic CMOS logic.	[L1] [CO4]	**[5M]**
6		Explain the following with an example.	[L2] [CO6]	**[10M]**
		(i) Domino CMOS logic. (ii) NORA logic.		
7	**a)**	Explain the criteria for choice of layers.	[L2] [CO6]	**[5M]**
	b)	Explain about complex logic gates.	[L2] [CO4]	**[5M]**
8		What is the necessity of floor planning concept in VLSI circuits? Discuss withsuitable example.	[L2] [CO5]	**[10M]**
9		What are the design methods used in physical design cycle? Explain each termwith suitable diagrams.	[L1] [CO4]	**[10M]**
10	**a)**	Discuss about the Power Estimation in CMOS circuit.	[L2] [CO5]	**[5M]**
	b)	Explain about Power delay estimation in VLSI circuits.	[L2] [CO5]	**[5M]**
11		Explain the following terms	[L2] [CO5]	**[10M]**
		(i) Floor planning (ii) Placement (iii) Routing		

UNIT –IV
SUBSYSTEM DESIGN

1	**a)**	Define the Counters in the digital circuit.	[L1] [CO4]	**[2M]**
	b)	What are the high-density memory elements? Explain in brief.	[L2] [CO5]	**[2M]**
	c)	Define Parity generator logic circuits.	[L1] [CO4]	**[2M]**
	d)	Define Comparator logic circuit.	[L1] [CO4]	**[2M]**
	e)	Differentiate Comparator and Magnitude Comparator.	[L2] [CO4]	**[2M]**
2		Explain different adder designs in sub circuit design with neat sketches.	[L2] [CO4]	**[10M]**
3	**a)**	What is shifter? List the types of shift registers and explain.	[L1 & L2] [CO4]	**[5M]**
	b)	Construct and explain the operation of shifter implemented by full adder.	[L3 & L2] [CO4]	**[5M]**
4		Explain the following logic circuit.	[L2] [CO4]	**[10M]**
		(i) Parity Generator (ii) Comparator.		
5		Design an Arithmetic and Logic Unit circuit with four functions using multiplexers and explain its operation.	[L6] [CO4]	**[10M]**
6	**a)**	Compare different types of memory elements.	[L2] [CO4]	**[5M]**
	b)	Develop the 4x4 array multiplier.	[L3] [CO4]	**[5M]**
7	**a)**	Explain the working of Zero/one detector implemented with adder circuit.	[L2] [CO4]	**[6M]**
	b)	List the advantages and applications of Zero/one detector.	[L1] [CO4]	**[4M]**
8		Summarize the following.	[L2] [CO4]	**[10M]**
		(i) Unsigned magnitude comparator. (ii) Asynchronous Counters.		
9	**a)**	Construct and explain the circuit diagram of 3-bit LFSR with example.	[L3] [CO4]	**[5M]**
	b)	Construct and explain the Johnson counter.	[L3] [CO4]	**[5M]**
10	**a)**	Construct and explain the circuit diagram of 4-bit Ripple Carry Adder.	[L3] [CO4]	**[5M]**
	b)	Construct and explain the ripple counter.	[L3] [CO4]	**[5M]**
11	**a)**	Explain about 4 transistor Dynamic memory cell.	[L2] [CO4]	**[5M]**
	b)	Explain about 6 transistor Static memory cell.	[L2] [CO4]	**[5M]**

UNIT –V
SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN AND CMOS TESTING

1	**a)**	Classify PLD.	[L2] [CO6]	**[2M]**
	b)	What is the need of Testing?	[L1] [CO6]	**[2M]**
	c)	Differentiate FPGA and CPLD.	[L2] [CO6]	**[2M]**
	d)	Explain what are the test principles available for the VLSI testing?	[L2] [CO6]	**[2M]**
	e)	Enumerate the advantages of CPLD.	[L1] [CO6]	**[2M]**
	f)	List the Boundary Scan Standards.	[L1] [CO6]	
2	**a)**	Compare PROM, PAL, and PLA with an example.	[L2] [CO6]	**[5M]**
	b)	Design the PAL Structure for the Boolean function **f1(a,b,c,d)=ab+bc & f2(a,b,c,d)=ab+cd**.	[L6] [CO6]	**[5M]**
3	**a)**	Illustrate the architecture of FPGA with neat sketch.	[L2] [CO6]	**[5M]**
	b)	Discuss about the merits of FPGA over other PLD architectures.	[L2] [CO6]	**[5M]**
4	**a)**	Describe about CPLD structure in detail and explain each block.	[L1] [CO6]	**[5M]**
	b)	Generalize the design approach for VSLI system design.	[L2] [CO6]	**[5M]**
5		Design the following functions in PLA structure.	[L6] [CO6]	**[10M]**
		(i) Y1=A'B'C'+ABC+A'B+ABC'		
		(ii) Y2=ABC+A'B'C+AC		
		(iii) Y3=A'BC'+AB'C+B'C'		
6	**a)**	Explain in detail about standard cell design with suitable diagrams.	[L2] [CO6]	**[5M]**
	b)	Give examples of various fault models available for VLSI testing?	[L2] [CO6]	**[5M]**
7	**a)**	What is the need for testing? Explain about Fault simulation.	[L1] [CO6]	
	b)	Give a logic circuit example in which stuck-at-1 fault and stuck-at-0 fault are indistinguishable.	[L2] [CO6]	**[5M]**
8	**a)**	What is FPGA. Draw and explain basic structure of FPGA.	[L2] [CO6]	**[5M]**
	b)	Discuss about the Fault coverage and how to find it?	[L1] [CO6]	**[5M]**
9		Explain Chip Level Test techniques and its methodology.	[L2] [CO6]	**[5M]**
10	**a)**	What is testing? Explain any three test principles.	[L1] [CO6]	**[10M]**
	b)	What is controllability and observability? Give examples to explain it.	[L2] [CO6]	**[5M]**
11		What is BILBO? Draw the logic diagram of BILBO & explain itsoperation in different modes?	[L1 & L2] [CO6]	**[10M]**

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